

## **REMARKS**

The Final Office Action dated July 30, 2004, has been received and reviewed.

Claims 1-3, 5-41, and 43-55 remain pending and under consideration in the above-referenced application. Each of claims 1-3, 5-41, and 43-55 stands rejected.

Reconsideration of the above-referenced application is respectfully requested.

### **Rejections Under 35 U.S.C. § 103(a)**

Each of claims 1-3, 5-41, and 43-55 has been rejected under 35 U.S.C. § 103(a).

The standard for establishing and maintaining a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.  
*In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

### Kim and Lin

Claims 1-3, 5-10, 15, 18, 19, 21, 22, 26- 28, 30- 36, 43, 44, and 50-52 stand rejected under 35 U.S.C. § 103(a) for being drawn to subject matter which is purportedly unpatentable over the subject matter taught in U.S. Patent 6,004,867 to Kim et al. (hereinafter "Kim"), in view of teachings from U.S. Patent 5,258,648 to Lin (hereinafter "Lin").

The teachings of Kim are drawn to substrates that include conductive traces that are carried either internally within the substrate (col. 3, line 55) or on a surface that is to be disposed against a semiconductor die (FIGs. 1 and 2).

While Kim teaches that the conductive traces may be located anywhere *in* the substrate (col. 3, line 55) or at a surface of the substrate which is to be disposed against the semiconductor die (FIGs. 1 and 2), Kim does not teach or suggest that the conductive traces may be carried upon

the opposite, exposed surface of the substrate. Instead, the teachings of Kim are limited to a substrate with conductive traces that are carried by the surface that is to be positioned against a semiconductor device.

Lin teaches a composite flip chip semiconductor device. Col. 1, lines 28-31. The semiconductor device of Lin lacks a conventional package body, minimizing the size thereof. Col. 1, lines 52-54. The semiconductor device of Lin includes an interposer with conductive traces that are carried on a surface that is to be positioned against the active surface of a semiconductor die. FIGs. 1 and 5E.

Lin lacks any teaching or suggestion that a second surface of the interposer thereof, which is to be located opposite the semiconductor die, may carry at least one conductive trace.

It is respectfully submitted that there are several reasons that the teachings of Kim and Lin do not support a *prima facie* case of obviousness under 35 U.S.C. § 103(a) against any of claims 1-3, 5-10, 15, 18, 19, 21, 22, 26-28, 30-36, 43, 44, or 50-52.

*Kim and Lin Do Not Teach or Suggest Each and Every Claim Element*

First, it is respectfully submitted that Kim and Lin, taken either separately or together, do not teach or suggest each and every element of any of claims 1-3, 5-10, 15, 18, 19, 21, 22, 26-28, 30-36, 43, 44, or 50-52.

Independent claim 1, as proposed to be amended, recites a chip-scale package which includes a semiconductor device and a substrate with a first surface disposed adjacent an active surface of the semiconductor device. At least one electrically conductive via extends at least partially through the substrate to communicate with a corresponding bond pad of the semiconductor device. The substrate also includes a second surface, which is opposite from the first surface, which carries at least one conductive trace, which communicates with the at least one conductive via.

In contrast to the subject matter recited in amended independent claim 1, Kim and Lin, taken either separately or together, lack any teaching or suggestion of a chip-scale package with an interposer that includes conductive traces that communicate with conductive vias thereof and

that are carried upon a surface which is opposite the surface adjacent to which a semiconductor device is positioned.

As Kim and Lin do not teach or suggest each and every element of amended independent claim 1, it is respectfully submitted that a *prima facie* case of obviousness has not been established against amended independent claim 1. Therefore, under 35 U.S.C. § 103(a), the subject matter to which amended independent claim 1 is directed is allowable over the subject matter taught in Kim and Lin.

Claims 2, 3, 5-10, 15, 18, and 19 are each allowable, among other reasons, for depending either directly or indirectly from claim 1, which is allowable.

Independent claim 21, as proposed to be amended, is directed to a chip-scale package with a substrate with first and second surfaces and a semiconductor device invertedly disposed adjacent to the first surface of the substrate. The first surface of the substrate includes contact areas that correspond to an arrangement of bond pads on the semiconductor device. An opposite, second surface of the substrate carries at least one conductive trace.

Again, Kim and Lin, taken either individually or collectively, do not teach a substrate which includes a first surface, adjacent to which a semiconductor device is secured, and an opposite, second surface that carries at least one conductive trace. Therefore, these references cannot be relied upon to establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a) against amended independent claim 21.

Each of claims 22, 26-28, and 30-36 is allowable, among other reasons, for depending either directly or indirectly from claim 21, which is allowable.

Turning now to independent claim 43, as proposed to be amended, it is directed to a carrier with at least one via that extends from a first surface of the carrier, adjacent to which a semiconductor device is to be positioned, to an opposite, second surface of the carrier. At least one conductive trace, which extends laterally from an end of the via, is carried by the second surface of the carrier.

Neither Kim nor Lin, taken either separately or together, teaches or suggests an interposer with a first surface that is to be positioned adjacent a semiconductor device and an opposite, second surface that carries at least one conductive trace.

Therefore, it is respectfully submitted that, under 35 U.S.C. § 103(a), a *prima facie* case of obviousness has not been set forth against amended independent claim 43. Under 35 U.S.C. § 103(a), amended independent claim 43, therefore, recites subject matter which is allowable over the combined teachings of Kim and Lin.

Claims 44 and 50-52 are each allowable, among other reasons, for depending either directly or indirectly from claim 43.

*There Is No Motivation to Combine the Teachings of Kim and Lin in the Asserted Manner*

Second, it is respectfully submitted that a *prima facie* case of obviousness under 35 U.S.C. § 103(a) has not been established because one of ordinary skill in the art would not have been motivated to combine the teachings of Kim and Lin in the manner that has been asserted.

Specifically, neither Kim nor Lin teaches or suggests an interposer with conductive traces that are carried upon an exposed surface thereof (*i.e.*, by an opposite surface from that adjacent to which a semiconductor device is to be positioned). Thus, neither of these references could provide one of ordinary skill in the art with any motivation to combine their teachings in a manner that would render the subject matter recited in any of claims 1-3, 5-10, 15, 18, 19, 21, 22, 26-28, 30-36, 43, 44, or 50-52 obvious.

Moreover, neither Kim nor Lin, when viewed individually or collectively, would have provided one or ordinary skill in the art with any suggestion or motivation to place a conductive trace of the interposer from Lin on the surface of the substrate of Kim that faces away from the semiconductor device of Kim in order to arrive at the chip-scale package of amended independent claim 1. As stated in Kim “[t]he electrically conductive traces 122 can be freely patterned **in** the substrate 120.” Col. 3, lines 16-17 (emphasis added). Kim further states, “after the substrate 320 is firmly attached to the wafer 300, a substrate-wafer-composite 390 is formed. The top surface of the substrate 320 is back-lapped so that the terminal pads 324 **in** the

substrate 320 are exposed.” Col. 6, lines 16-21 (emphasis added); *see also*, FIG. 5D.

Nonetheless, Kim lacks any teaching or suggestion that conductive traces may be exposed during the back-lapping process. Moreover, the conductive traces of the substrate of Kim perform the function of routing the vias to other electrical connections; therefore, the addition of traces to the surface would increase the cost of manufacturing the devices, which is contrary to a stated object of Kim. *See*, col. 1, lines 49-51.

It appears that any motivation to combine the teachings of Kim and Lin in the manner that has been asserted could only have been improperly gleaned from the hindsight provided by the disclosure of the above-referenced application.

Without a suggestion or motivation to combine the teachings of Kim and Lin, a *prima facie* case of obviousness cannot be established against any of claims 1-3, 5-10, 15, 18, 19, 21, 22, 26-28, 30-36, 43, 44, or 50-52 under 35 U.S.C. § 103(a).

#### *There Is No Reasonable Expectation of Success*

Third, since neither Kim nor Lin teaches or suggest an interposer with conductive traces that are carried by a surface which will not face a semiconductor device, one of ordinary skill in the art would have had no reason to expect that the teachings of these references could have been successfully combined in such a way as to come up with a semiconductor device that includes an interposer with conductive traces on a surface that faces away from a semiconductor device.

Therefore, a *prima facie* case of obviousness under 35 U.S.C. § 103(a) has not been established against any of claims 1 through 3, 5 through 10, 15, 18, 19, 21, 22, 26 through 28, 30 through 36, 43, 44, or 50 through 52.

#### Kim, Lin, and Gnadinger

Claims 11-14, 20, 23-25, 37-41, and 45-49 have been rejected under 35 U.S.C. § 103(a) for reciting subject matter which is allegedly unpatentable over teachings from Kim, in view of teachings from Lin and, further, in view of the subject matter taught in U.S. Patent 5,229,647 to Gnadinger (hereinafter “Gnadinger”).

Each of claims 11-14 and 20 is allowable, among other reasons, for depending either directly or indirectly from claim 1.

Claims 23-25 and 37-41 are each allowable, among other reasons, for depending either directly or indirectly from claim 21.

Claims 45-49 are each allowable, among other reasons, for depending either directly or indirectly from claim 43.

It is further submitted that a *prima facie* case of obviousness under 35 U.S.C. § 103(a) cannot be established with regard to any of claims 11-14, 20, 23-25, 37-41, or 45-49 since no suggestion or motivation exists to combine teachings from Gnadinger with the teachings of either Kim or Lin. Gnadinger, which discloses wafers having vias extending completely therethrough, like Kim and Lin, lacks any teaching or suggestion of substrates with conductive traces on the surfaces thereof that are to face away, or be located opposite, from a semiconductor device with which the substrates are to be assembled.

Additionally, Gnadinger does not include any teaching or suggestion that would provide one of ordinary skill in the art with a reason to expect the combination of teachings from Kim, Lin, and Gnadinger to be successful.

Thus, a *prima facie* case of obviousness cannot be established for any of claims 11-14, 20, 23-25, 37-41, or 45-49 under 35 U.S.C. § 103(a).

#### Kim, Lin, and Higgins

Claims 16, 17, 29, and 53-55 stand rejected under 35 U.S.C. § 103(a) for being directed to subject matter which is assertedly unpatentable over the teachings of Kim, in view of the subject matter taught in Lin and, further, in view of the teachings of U.S. Patent 6,294,405 to Higgins, III (hereinafter “Higgins”).

Claims 16 and 17, 29, and 53- 55 are each allowable, among other reasons, for depending from claims 1, 21, and 43, respectively, each of which is allowable.

Furthermore, Higgins teaches a sub-chip-scale package having a substrate electrically connected to a semiconductor device, but, like Kim and Lin, lacks any teaching or suggestion of conductive traces on a surface of the substrate that is opposite the semiconductor device and,

thus, the resultant combination of Higgins with Kim and Lin does not remedy the aforementioned deficiencies of Kim and Lin as required to establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a).

Thus, a *prima facie* case of obviousness cannot be established against any of claims 16, 17, 29 or 53-55 under 35 U.S.C. § 103(a).

In view of the foregoing, withdrawal of the 35 U.S.C. § 103(a) rejections of claims 1-3, 5-41, and 43-55 is respectfully requested.

**ENTRY OF AMENDMENTS**

It is respectfully requested that the proposed claim amendments be entered because the proposed amendments place the above-referenced application in condition for allowance and are timely filed.

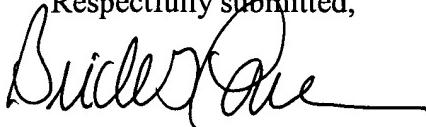
The proposed amendments do not introduce new matter into the application, nor would they require an additional search. Further, the proposed claim amendments do not alter the scope of any of the amended claims; they have been made solely for the purpose of identifying the relationships between different elements with improved clarity.

In the event that a decision is made not to enter the proposed claim amendments, entry thereof upon the filing of a Notice of Appeal in the above-referenced application is respectfully requested.

**CONCLUSION**

It is respectfully submitted that each of claims 1-3, 5-41, and 43-55 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,



Brick G. Power  
Registration No. 38,581  
Attorney for Applicant  
TRASKBRITT, PC  
P.O. Box 2550  
Salt Lake City, Utah 84110-2550  
Telephone: 801-532-1922

Date: September 30, 2004

BGP/dlm:rmh  
Document in ProLaw